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| 09/989,317 | 11/20/2001 | Xavier Mariaud | 00RO27054366 | 9505 |

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| EXAMINER | |
|---|---|
| LEE, CHRISTOPHER E | |
| **ART UNIT** | **PAPER NUMBER** |
| 2112 | |

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application N . | Applicant(s) | |
|---|---|---|---|
| | 09/989,317 | MARIAUD ET AL. | |
| | Examiner | Art Unit | |
| | Christopher E. Lee | 2112 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Peri d for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *5-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Receipt Acknowledgement*

1. Receipt is acknowledged of the Amendment filed on 15th of October 2004. Claims 5, 7, 11, 12, 17; 20 and 22 have been amended; no claim has been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 10th of June 2004. Currently, claims 5-22 are pending in this application.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 5-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art [hereinafter AAPA] in view of Shiroshita et al. [US 5,892,894 A; hereinafter Shiroshita].

*Referring to claim 5,* AAPA discloses a computer system (See Fig. 1) comprising: a master apparatus (i.e., Master Apparatus A in Fig. 1); and a slave apparatus (i.e., Slave Apparatus B in Fig. 1) for communicating with said master apparatus (See page 1, lines 10-22) and communicating via a universal serial bus (USB) protocol (See page 1, lines 22-25), said slave apparatus comprising a sending/receiving

circuit (i.e., Send/Receive device 24 of Fig. 1) for sending and receiving binary information to and from said master apparatus (See page 1, line 25 through page 2, line 3; i.e., receiving a message from Master Apparatus, and responding acknowledge signal ACK to Master Apparatus) and supplying status signals based thereon (e.g., supplying Setup, CTR and End_trans signals shown in Fig. 3), a plurality of state latches (e.g., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) and control circuitry (e.g., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) cooperating therewith for receiving said status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon (See page 7, line 18 through page 8, line 7), a microprocessor (i.e., Microcontroller 28 of Fig. 1) for processing applications of said slave apparatus (See page 2, lines 8-13; i.e., wherein in fact that the microcontroller of the slave apparatus has to perform more and more tasks inherently anticipates a processor for processing applications of said slave apparatus) and also for processing said binary information received by said sending/receiving circuit (See page 3, lines 14-26; i.e., wherein in fact that an interruption of the microcontroller to process the part of the transmitted message may be requested inherently anticipates a processor for processing said binary information received by said sending/receiving circuit), and an interruption state latch (i.e., a flag CTR in Fig. 3(d)) and a control circuit (i.e., means for controlling said flag CTR in Fig. 3(d)) cooperating therewith for supplying an interruption signal (i.e., an interruption when CTR is set to '1' in Fig. 3(d)) once the start of a new message (e.g., message including SETUP and DATA in the phase 10 of Fig. 3(a)) has been acknowledged (i.e., said CTR being set after ACK in the phase 10 of Fig. 3(a)) and recorded by said sending/receiving circuit (See page 3, lines 20-26; i.e., wherein in fact that a software state machine then processes the information concerning the event of the USB message extracted by the interrupt routine implies that said sending/receiving circuit records said new message (i.e., USB message) for processing the information concerning the event of said message later by said software state machine).

AAPA does not teach said supplying said interruption signal is performed when said microprocessor is unavailable.

Shiroshita discloses a data re-transmission management scheme (See Fig. 4 and Abstract), wherein supplying an interruption signal (i.e., busy notification S101 in Fig. 8) when a microprocessor is unavailable (i.e., busy terminal; See col. 6, lines 34-38).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data re-transmission management scheme, as disclosed by Shiroshita, in said interruption state latch and said circuit cooperating therewith, as disclosed by AAPA, for the advantage of providing said data re-transmission management scheme capable of improving said communication efficiency, by carrying out the data sending (i.e., transmission) and resending (i.e., re-transmission) with respect to normal slave apparatus first, and carrying out the data sending (i.e., transmission) and resending (i.e., re-transmission) with respect to slave apparatus, in which a microprocessor is unavailable (i.e., busy status; See Shiroshita, col. 2,.lines 50-58).

*Referring to claim 6,* AAPA teaches said control circuit (i.e., means for controlling said flag CTR in Fig. 3(d)) for controlling said interruption state latch (See page 3, lines 14-26) comprises at least one logic circuit (i.e., means for switching/latching signals between "1" and "0" for Setup, CTR and End_trans signals in Fig. 3) for receiving said status signals (i.e., Setup, CTR and End_trans signals shown in Fig. 3) from said sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) and setting said interruption state latch (i.e., the flag CTR in Fig. 3(d)) to a predetermined logic level (i.e., the logic '1' state) to indicate a microprocessor interruption request (See page 3, lines 14-18).

*Referring to claim 7,* AAPA teaches said control circuitry (i.e., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) for controlling said state latches (i.e., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) prevents said binary information from said sending/receiving circuit (i.e., message from Master Apparatus via Send/Receive device; See page 1, line

25 through page 2, line 3) from being written into said plurality of state latches during receipt of the start of said new message and during the presence of said interruption signal (See phases 12 and 14 in Fig. 3, and page 3, lines 14-29; i.e., wherein in fact that no transfer over the USB bus is authorized during CTR being set to '1' inherently anticipates said control circuitry prevents the binary information from being written into said plurality of state latches during receipt of the start of said new message and during the presence of said interruption signal).

*Referring to claim 8,* AAPA teaches said master apparatus (i.e., Master Apparatus A in Fig. 1) comprises a central processing unit (i.e., Microcontroller 26 of Fig. 1).

*Referring to claim 9,* AAPA teaches said slave apparatus (i.e., Slave Apparatus B in Fig. 1) comprises computer peripheral device (See page 1, line 3-5).

*Referring to claim.10,* AAPA teaches a cable (i.e., cable 20 of Fig. 1) connecting said master apparatus and said slave apparatus (See page 1, lines 10-19).

*Referring to claim 11,* AAPA discloses a computer system (See Fig. 1) comprising: a master apparatus (i.e., Master Apparatus A in Fig. 1); and a slave apparatus (i.e., Slave Apparatus B in Fig. 1) for communicating with said master apparatus (See page 1, lines 10-22) and comprising a sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) for sending and receiving binary information to and from said master apparatus (See page 1, line 25 through page 2, line 3; i.e., receiving a message from Master Apparatus, and responding acknowledge signal ACK to Master Apparatus) and supplying status signals based thereon (e.g., supplying Setup, CTR and End_trans signals shown in Fig. 3), a plurality of state latches (e.g., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) and control circuitry (e.g., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) cooperating therewith for receiving said status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon (See page 7, line 18 through page 8, line 7), a microprocessor (i.e., Microcontroller 28 of Fig. 1) for processing applications of said slave apparatus (See

page 2, lines 8-13; i.e., wherein in fact that the microcontroller of the slave apparatus has to perform more and more tasks inherently anticipates a processor for processing applications of said slave apparatus) and also for processing said binary information received by said sending/receiving circuit (See page 3, lines 14-26; i.e., wherein in fact that an interruption of the microcontroller to process the part of the transmitted message may be requested inherently anticipates a processor for processing said binary information received by said sending/receiving circuit), and an interruption state latch (i.e., a flag CTR in Fig. 3(d)) for supplying an interruption signal (i.e., an interruption when CTR is set to '1' in Fig. 3(d)) once the start of a new message (e.g., message including SETUP and DATA in the phase 10 of Fig. 3(a)) has been acknowledged (i.e., said CTR being set after ACK in the phase 10 of Fig. 3(a)) and recorded by said sending/receiving circuit (See page 3, lines 20-26; i.e., wherein in fact that a software state machine then processes the information concerning the event of the USB message extracted by the interrupt routine implies that said sending/receiving circuit records said new message (i.e., USB message) for processing the information concerning the event of said message later by said software state machine), said control circuitry (i.e., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) for controlling said state latches (i.e., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) preventing said binary information from said sending/receiving circuit (i.e., message from Master Apparatus via Send/Receive device; See page 1, line 25 through page 2, line 3) from being written into said plurality of state latches during receipt of the start of said new message and during the presence of said interruption signal (See phases 12 and 14 in Fig. 3, and page 3, lines 14-29; i.e., wherein in fact that no transfer over the USB bus is authorized during CTR being set to '1' inherently anticipates said control circuitry prevents the binary information from being written into said plurality of state latches during receipt of said start of said new message and during the presence of said interruption signal).

AAPA does not teach said supplying said interruption signal is performed when said microprocessor is unavailable.

Shiroshita discloses a data re-transmission management scheme (See Fig. 4 and Abstract), wherein supplying an interruption signal (i.e., busy notification S101 in Fig. 8) when a microprocessor is unavailable (i.e., busy terminal; See col. 6, lines 34-38).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data re-transmission management scheme, as disclosed by Shiroshita, in said interruption state latch and said circuit cooperating therewith, as disclosed by AAPA, for the advantage of providing said data re-transmission management scheme capable of improving said communication efficiency, by carrying out the data sending (i.e., transmission) and resending (i.e., re-transmission) with respect to normal slave apparatus first, and carrying out the data sending (i.e., transmission) and resending (i.e., re-transmission) with respect to slave apparatus, in which a microprocessor is unavailable (i.e., busy status; See Shiroshita, col. 2, lines 50-58).

*Referring to claim 12,* AAPA teaches said master apparatus and said slave apparatus communicate via a universal serial bus (USB) protocol (See page 1, lines 22-25).

*Referring to claim 13,* AAPA teaches at least one logic circuit (i.e., means for switching/latching signals between "1" and "0" for Setup, CTR and End_trans signals in Fig. 3) for receiving said status signals (i.e., Setup, CTR and End_trans signals shown in Fig. 3) from said sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) and setting said interruption state latch (i.e., the flag CTR in Fig. 3(d)) to a predetermined logic level (i.e., the logic '1' state) to indicate a microprocessor interruption request (See page 3, lines 14-18).

*Referring to claim 14,* AAPA teaches said master apparatus (i.e., Master Apparatus A in Fig. 1) comprises a central processing unit (i.e., Microcontroller 26 of Fig. 1).

*Referring to claim 15,* AAPA teaches said slave apparatus (i.e., Slave Apparatus B in Fig. 1) comprises computer peripheral device (See page 1, line 3-5).

*Referring to claim 16,* AAPA teaches a cable (i.e., cable 20 of Fig. 1) connecting said master apparatus and said slave apparatus (See page 1, lines 10-19).

*Referring to claim 17,* AAPA discloses a slave apparatus (i.e., Slave Apparatus B in Fig. 1) for communicating with a master apparatus (i.e., Master Apparatus A in Fig. 1; See page 1, lines 10-22) via a universal serial bus (USB) protocol (See page 1, lines 22-25), said slave apparatus comprising: a sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) for sending and receiving binary information to and from said master apparatus (See page 1, line 25 through page 2, line 3; i.e., receiving a message from Master Apparatus, and responding acknowledge signal ACK to Master Apparatus) and supplying status signals based thereon (e.g., supplying Setup, CTR and End_trans signals shown in Fig. 3); a plurality of state latches (e.g., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) and control circuitry (e.g., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) cooperating therewith for receiving said status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon (See page 7, line 18 through page 8, line 7); a microprocessor (i.e., Microcontroller 28 of Fig. 1) for processing applications of said slave apparatus (See page 2, lines 8-13; i.e., wherein in fact that the microcontroller of the slave apparatus has to perform more and more tasks inherently anticipates a processor for processing applications of said slave apparatus) and also for processing said binary information received by said sending/receiving circuit (See page 3, lines 14-26; i.e., wherein in fact that an interruption of the microcontroller to process the part of the transmitted message may be requested inherently anticipates a processor for processing said binary information received by said sending/receiving circuit); and an interruption state latch (i.e., a flag CTR in Fig. 3(d)) and a control circuit (i.e., means for controlling said flag CTR in Fig. 3(d)) cooperating therewith for supplying an interruption signal (i.e., an interruption when CTR is set to '1' in Fig. 3(d)) once the start of a new message (e.g., message including SETUP and DATA in the phase 10 of Fig. 3(a)) has been acknowledged (i.e., said CTR being set after ACK in the phase 10 of Fig. 3(a)) and recorded by

said sending/receiving circuit (See page 3, lines 20-26; i.e., wherein in fact that a software state machine then processes the information concerning the event of the USB message extracted by the interrupt routine implies that said sending/receiving circuit records said new message (i.e., USB message) for processing the information concerning the event of said message later by said software state machine). AAPA does not teach said supplying said interruption signal is performed when said microprocessor is unavailable.

Shiroshita discloses a data re-transmission management scheme (See Fig. 4 and Abstract), wherein supplying an interruption signal (i.e., busy notification S101 in Fig. 8) when a microprocessor is unavailable (i.e., busy terminal; See col. 6, lines 34-38).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data re-transmission management scheme, as disclosed by Shiroshita, in said interruption state latch and said circuit cooperating therewith, as disclosed by AAPA, for the advantage of providing said data re-transmission management scheme capable of improving said communication efficiency, by carrying out the data sending (i.e., transmission) and resending (i.e., re-transmission) with respect to normal slave apparatus first, and carrying out the data sending (i.e., transmission) and resending (i.e., re-transmission) with respect to slave apparatus, in which a microprocessor is unavailable (i.e., busy status; See Shiroshita, col. 2, lines 50-58).

*Referring to claim 18,* AAPA teaches said control circuit (i.e., means for controlling said flag CTR in Fig. 3(d)) for controlling said interruption state latch (See page 3, lines 14-26) comprises at least one logic circuit (i.e., means for switching/latching signals between "1" and "0" for Setup, CTR and End_trans signals in Fig. 3) for receiving said status signals (i.e., Setup, CTR and End_trans signals shown in Fig. 3) from said sending/receiving circuit (i.e., Send/Receive device 24 of Fig. 1) and setting said interruption state latch (i.e., the flag CTR in Fig. 3(d)) to a predetermined logic level (i.e., the logic '1' state) to indicate a microprocessor interruption request (See page 3, lines 14-18).

*Referring to claim 19,* AAPA teaches said control circuitry (i.e., Multiplexers 38R0, 38R1 or 38T0, 38T1 in Fig. 2) for controlling said state latches (i.e., D-type state latches 32R0, 32R1 or 32T0, 32T1 in Fig. 2; See page 6, line 33 through page 7, line 3) prevents said binary information from said sending/receiving circuit (i.e., message from Master Apparatus via Send/Receive device; See page 1, line 25 through page 2, line 3) from being written into said plurality of state latches during receipt of the start of said new message and during the presence of said interruption signal (See phases 12 and 14 in Fig. 3, and page 3, lines 14-29; i.e., wherein in fact that no transfer over the USB bus is authorized during CTR being set to '1' inherently anticipates said control circuitry prevents the binary information from being written into said plurality of state latches during receipt of the start of said new message and during the presence of said interruption signal).

*Referring to claim 20,* AAPA discloses a method of processing interruptions (See page 3, lines 14-26) in a slave apparatus (i.e., Slave Apparatus B in Fig. 1) communicating with a master apparatus (i.e., Master Apparatus A in Fig. 1) via a universal serial bus (USB) protocol (See page 1, lines 22-25), said method comprising: sending and receiving binary information to and from said master apparatus via a sending/receiving circuit (See page 1, line 25 through page 2, line 3; i.e., receiving a message from Master Apparatus, and responding acknowledge signal ACK to Master Apparatus) and supplying status signals based thereon (e.g., supplying Setup, CTR and End_trans signals shown in Fig. 3); generating state signals of said sending/receiving circuit based upon said status signals (See page 7, line 18 through page 8, line 7); processing applications of said slave apparatus (i.e., SW Process 'main routine' in Fig. 3(e)) and also processing said binary information received by said sending/receiving circuit (See page 3, lines 24-26); and supplying an interruption signal (i.e., CTR being set to '1' in Fig. 3(d)) once the start of a new message (e.g., message including SETUP and DATA in the phase 10 of Fig. 3(a)) has been acknowledged (i.e., said CTR being set after ACK in the phase 10 of Fig. 3(a)) and recorded by said sending/receiving circuit (See page 3, lines 20-26; i.e., wherein in fact that a software state machine then

processes the information concerning the event of the USB message extracted by the interrupt routine implies that said sending/receiving circuit records said new message (i.e., USB message) for processing the information concerning the event of said message later by said software state machine).

AAPA does not teach said supplying said interruption signal is performed when said microprocessor is unavailable.

Shiroshita discloses a data re-transmission management scheme (See Fig. 4 and Abstract), wherein supplying an interruption signal (i.e., busy notification S101 in Fig. 8) when a microprocessor is unavailable (i.e., busy terminal; See col. 6, lines 34-38).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data re-transmission management scheme, as disclosed by Shiroshita, in said interruption state latch and said circuit cooperating therewith, as disclosed by AAPA, for the advantage of providing said data re-transmission management scheme capable of improving said communication efficiency, by carrying out the data sending (i.e., transmission) and resending (i.e., re-transmission) with respect to normal slave apparatus first, and carrying out the data sending (i.e., transmission) and resending (i.e., re-transmission) with respect to slave apparatus, in which a microprocessor is unavailable (i.e., busy status; See Shiroshita, col. 2, lines 50-58).

*Referring to claim 21,* AAPA teaches supplying said interruption signal comprises setting an interruption state latch (i.e., the flag CTR in Fig. 3(d)) to a predetermined logic level (i.e., the logic '1' state) based upon said status signals (i.e., Setup, CTR and End_trans signals shown in Fig. 3) to indicate a microprocessor interruption request (See page 3, lines 14-18).

*Referring to claim 22,* AAPA discloses a method of processing interruptions (See page 3, lines 14-26) in a slave apparatus (i.e., Slave Apparatus B in Fig. 1) communicating with a master apparatus (i.e., Master Apparatus A in Fig. 1) via a universal serial bus (USB) protocol (See page 1, lines 22-25), said method comprising: generating a state signal indicating the end of a message (See page 1, line 26

through page 2, line 6); detecting a start of a new message (i.e., message 'IN' signal in Fig. 3(a)) from said master apparatus (See page 2, lines 7-10) and producing a start of message state signal (i.e., 'ready' state signal); recording data from the start of said new message (See page 2, lines 13-17); acknowledging receipt of the start of said new message (i.e., ACK signal in Fig. 3(a)); generating a signal (i.e., flag CTR in Fig. 3(d)) indicating completion (i.e., CTR being set to '0' in Fig. 3(d)) of recordation of said data from the start of said new message (See page 3, lines 14-26); and generating an interruption signal (i.e., an interruption when CTR is set to '1' in Fig. 3(d)) in the presence of said state signal indicating the end of said message, the start of message state signal, and said signal indicating completion of recordation of said data from the start of said new message (See page 3, lines 14-16; i.e., wherein in fact that at the end of transfer phase, an interruption of the microcontroller to process the part of the transmitted message may be requested inherently anticipates generating an interruption signal in the presence of said state signal indicating the end of said message (i.e., CTR being set to '1'), the start of message state signal (i.e., 'ready' state signal), and said signal indicating completion of recordation of said data from the start of said new message).

AAPA does not teach said generating said interruption signal is performed when said microprocessor is unavailable.

Shiroshita discloses a data re-transmission management scheme (See Fig. 4 and Abstract), wherein generating an interruption signal (i.e., busy notification S101 in Fig. 8) when a microprocessor is unavailable (i.e., busy terminal; See col. 6, lines 34-38).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data re-transmission management scheme, as disclosed by Shiroshita, in said interruption state latch and said circuit cooperating therewith, as disclosed by AAPA, for the advantage of providing said data re-transmission management scheme capable of improving said communication efficiency, by carrying out the data sending (i.e., transmission) and resending (i.e., re-transmission) with

respect to normal slave apparatus first, and carrying out the data sending (i.e., transmission) and resending (i.e., re-transmission) with respect to slave apparatus, in which a microprocessor is unavailable (i.e., busy status; See Shiroshita, col. 2, lines 50-58).

***Response to Arguments***

5. Applicants' arguments with respect to claims 5, 11, 17, 20 and 22 have been considered but are moot in view of the new ground(s) of rejection.

*In response to the Applicants' arguments with respect to* "the interruption state latch and a control circuit cooperate for supplying an interruption signal once the start of a new message has been acknowledged and recorded by the sending/receiving circuit when the microprocessor is unavailable" in the claims 5, 11, 17, 20 and 22, respectively, the Examiner brought **Shiroshita** reference in the rejection for the limitations which are not provided by **AAPA** (See *Claim Rejections - 35 USC § 103*).

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sapir et al. [US 5,717,931 A] disclose method and apparatus for communicating between master and slave electronic devices where the slave device may be hazardous.

Lanctot [US 5,764,928 A] discloses microprocessor communication protocol in a multiprocessor transmitter.

Rice [US 6,195,721 B1] discloses inter-processor data transfer management.

7. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH

shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
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